**LISTING OF THE CLAIMS**:

Claim 1 (Currently Amended) A method of fabricating a semiconductor device comprising the steps of:

providing a structure comprising a carrier wafer, an oxide layer positioned on the carrier wafer, a polySi back-gate located on the oxide layer, a back-gate dielectric located on said polySi back-gate, and a Si-containing layer located on said back-gate dielectric;

forming a channel region into a portion of said Si-containing layer;

forming a front gate region comprising a front-gate dielectric, a front polySi gate and sacrificial spacers atop said channel region;

forming undercutting shallow trench isolation regions in said structure, wherein during said forming of said undercutting shallow trench isolation regions the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate;

removing the sacrificial spacers and forming source/drain extensions into the channel region; and

forming gate spacers atop the top of the channel region and source/drain regions in said channel region, wherein said polySi back-gate is self-aligned with the front polySi gate and the source/drain extensions.

Claim 2 (Original) The method of Claim 1 wherein said polySi back-gate is formed by implanting dopants into a polySi layer that is formed atop the back-gate dielectric and annealing the implanted dopants.

Claim 3 (Original) The method of Claim 1 wherein said back-gate dielectric is formed on the Si-containing layer of an initial silicon-on-insulator (SOI) substrate by a thermal growing process or deposition.

Claim 4 (Currently Amended) The method of Claim 1 wherein said ~~bonded~~ structure further includes deep trench isolation regions, each deep trench isolation region having an upper surface that is coplanar with an upper surface of the Si-containing layer.

Claim 5 (Currently Amended) The method of Claim 1 wherein said Si-containing layer of said ~~bonded~~ structure is thinned by a planarization process.

Claim 6 (Currently Amended) The method of Claim 1 wherein said ~~bonded~~ structure is formed by positioning said carrier wafer to be in contact with said oxide layer and performing a bonding step.

Claim 7 (Original) The method of Claim 6 wherein bonding step comprises heating at a temperature of from about 900° to about 1100°C for a time period of about 1.5 hours to about 2.5 hours.

Claim 8 (Original) The method of Claim 6 wherein said bonding step is performed at a temperature of from about 18° to about 27°C in the presence of an inert ambient.

Claim 9 (Original) The method of Claim 1 wherein said channel region is formed by ion implantation and annealing.

Claim 10 (Original) The method of Claim 9 wherein a sacrificial oxide layer is formed on the Si-containing layer prior to said ion implantation.

Claim 11 (Original) The method of Claim 1 wherein said sacrificial spacers have a width of from about 50 to about 100 nm.

Claim 12 (Original) The method of Claim 1 wherein said undercutting shallow trench isolation regions are formed by the steps of: chemical etching, isotropic reactive ion etching, oxidation and a second isotropic etch.

Claim 13 (Original) The method of Claim 1 wherein said sacrificial spacers are removed utilizing a chemical etchant.

Claim 14 (Original) The method of Claim 1 wherein said gate spacers are formed by deposition and etching.

Claim 15 (Original) The method of Claim 1 wherein said source/drain regions are formed by ion implantation and annealing using the gate spacers as an implant mask.

Claim 16 (Original) The method of Claim 1 further comprising forming raised source/drain regions on said source/drain regions, said raised source/drain regions are formed by deposition of an epi-Si or Si layer and ion implantation and annealing.

Claim 17 (Original) The method of Claim 16 further comprising forming silicide regions on said raised source/drain regions.

Claim 18 (Original) The method of Claim 17 further comprising forming an insulating layer having conductively filled contact holes atop the structure.

Claim 19 (New) A method of fabricating a semiconductor device comprising the steps of:

providing a structure comprising a carrier wafer, an oxide layer positioned on the carrier wafer, a polySi back-gate located on the oxide layer, a back-gate dielectric located on said polySi back-gate, and a Si-containing layer located on said back-gate dielectric;

forming a channel region into a portion of said Si-containing layer;

forming a front gate region comprising a front-gate dielectric, a front polySi gate and sacrificial spacers atop said channel region;

forming undercutting shallow trench isolation regions in said structure by the steps of chemical etching, isotropic reactive ion etching, oxidation and a second isotropic etch;

removing the sacrificial spacers and forming source/drain extensions into the channel region; and

forming gate spacers atop the top of the channel region and source/drain regions in said channel region, wherein said polySi back-gate is self-aligned with the front polySi gate and the source/drain extensions.